REMARKS

This Amendment "A" is submitted in response to the non-final Office Action dated December 11, 2003 (the "Office Action"), wherein pending claims 6 – 10, 12 and 14 were rejected as being anticipated by various prior art patents, and claims 11 and 13 were objected to as dependent on a rejected base claim. Claims 1 – 5 were previously withdrawn from consideration pursuant to a Restriction Requirement. By this Amendment, applicant has cancelled withdrawn claims 1 – 5, without prejudice, and has amended claims 6, 10 and 12. Claims 6 – 14 are pending. Reconsideration and reexamination of the application in view of the foregoing claim amendments and following remarks are respectfully requested.

Priority

Paragraph 2 of the Office Action states: "Acknowledgement is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d)." This appears to an error, as the applicants have made no claim for foreign priority. Paragraph 3 of the Office Action correctly notes that the present application is a continuation-in-part of U.S. Pat. App. Ser. No. 09/429,854. However, the examiner fails to acknowledge that the present application also claims priority, as a continuation-in-part, to U.S. Pat. App. Ser. No. 09/956,605.

Claim Amendments

Claim 6 was amended to clarify the structure being claimed, and to better differentiate the claimed subject matter from the prior art, as described in detail below. Claim 10 was amended to explicitly recite that the substrate is a semiconductor substrate, and that it is the sub-layer of the "first conductive layer" that is different than the adjacent material in the via which constitutes the second conductive material. Claim 12 was reworded for clarity.

Traversal of Rejections

Ozawa, et al.

Claim 6 was rejected under 35 U.S.C. § 102(e) as being anticipated by Ozawa et al., U.S. Pat. No. 6,316,838 ("Ozawa"). Ozawa shows a multichip module comprising several stacked IC "chips". A key part of this rejection is the examiner's contention that the Ozawa's substrate 33 is the "interconnect structure" of claim 6. In order to overcome this rejection, claim 6 has been

amended to recite that the "interconnect structure" is a "a multilayer thin-film polymeric interconnect structure." Ozawa's substrate 33 is not a "multilayer thin-film polymeric" interconnect structure and, therefore, does not meet the requirement of claim 6, as amended. Because Ozawa and the present application are commonly owned, Ozawa cannot be used in a § 103 rejection and, accordingly, it is unnecessary for applicant to discuss in detail why Ozawa does not make claim 6 obvious. Nonetheless, applicant submits that the Ozawa structure is significantly different than the structure set forth in claim 6 and, therefore, even if it could be used in an § 103 combination, it has no bearing on the obviousness of the claimed structure.

Kurashima, et al.

Claims 6 – 9 were rejected under § 102(e) over Kurashima, et al., U.S. Pat. No. 6,608,371 ("Kurashima"). Kurashima discloses a method of stacking IC chips, with insulating layers being disposed on the chips. However, Kurashima's insulating layers 22 are not "multilayer thin-film polymeric interconnect structures" as required by claim 6, as amended. Insulating layers 22 are used to electrically isolate the chips, not to serve as interconnect substrates.

The examiner appears to take the position that the language at column 16, lines 10, *et seq.*, of Kurashima, which states: "the 'semiconductor chip' could be replaced with 'electronic element'" such as a "capacitor", anticipates claim 7. Applicant points out that claim 7 requires that the semiconductor layer *includes* a capacitor and, therefore, a device which "replaces" a semiconductor chip with a capacitor does not meet the requirement of claim 7. There is no way to read the quoted language from Kurashima as disclosing a semiconductor which *includes* a capacitor.

Rostoker, et al.

Claims 10, 12 and 14 were rejected as being anticipated by Rostoker et al., U.S. Pat. No. 5,640,049 ("Rostoker"). Applicant respectfully traverses this rejection. Rostoker shows a semiconductor chip mounted on a substrate (which also may incorporate a semiconductor layer). Thus, there are two structures shown in Rostoker, as described, for example in the "Abstract" of the patent as follows:

> "An integrated circuit structure is described wherein *individual integrated circuit devices* such as MOS or bipolar transistors are constructed on and in a semiconductor substrate and one or more layers of metal interconnects are

constructed on and in a second substrate, preferably of similar thickness, and the ***two substrates*** are then aligned and bonded together to thereby provide electrical interconnections of individual integrated circuit devices on the semiconductor substrate with appropriate metal interconnects on the second substrate ..." (Emphasis added.)

And the "Detailed Description" states:

"The invention comprises an integrated circuit structure and process wherein individual integrated circuit devices such as MOS or bipolar transistors are constructed on and in a semiconductor substrate and one or more layers of metal interconnects are constructed on and in a second substrate, preferably of similar thickness, and the ***two substrates*** are then aligned and bonded together to thereby provide electrical interconnections of individual integrated circuit devices on the semiconductor substrate with appropriate metal interconnects on the second substrate to provide the desired integrated circuit structure ..." (Col. 4, line 65 – col. 5, line 8; emphasis added.)

Thus, it is clear that the Rostoker patent describes a structure made from two separate substrates, specifically, Rostoker describes one or more IC chips mounted on a carrier substrate. (See, *e.g.*, FIG. 16.) The examiner uses elements from both of these two substrates to find invention the elements described in claim 10. For example, the examiner states that the "first dielectric layer" is layer 320 which is found on the semiconductor chip, and that the second dielectric layer is layers 190 – 230, which are found on the second substrate. Applicant submits that this combination of elements from two separate substrates is improper. Claim 10 is directed to a structure formed on a *single* substrate. Accordingly, Rostoker does not anticipate claim 10, or any claim dependent thereon.

Claim 10 requires the presence of, "an aperture formed in the second layer and disposed over the first conductive layer *to expose a portion thereof,*" (emphasis added). This recited structure is not present in the combined substrates of Rostoker. Specifically, to the extent there is an aperture in the "second dielectric layer" which, according to the examiner, is on the second of Rostoker's substrates, the aperture does not "expose" any portion of the "first conductive layer" which, according to the examiner, is on the first of Rostoker's substrates. Thus, the "first conductive layer" (said to be 330-334) is at the uppermost surface of the first substrate and is fully exposed at all times. The formation of an aperture in the bottom dielectric layer of the second substrate plays no role in "exposing" any portion of the first conductive layer. The examiner is not free to ignore this claim requirement.

Claim 10 further requires that the second conductive material in a via which is "different from said first conductive material." Applicant found nothing in Rostoker which specifies that the first and second conductive materials be different. Contact between is made between "alloyable metal" 340/344 (which the examiner asserts is part of the first conductive layer) and "alloyable metal" 214/216, (which the examiner asserts is the second conductive material). There is no suggestion that these two "alloyable metal" are different, as required by claim 10. Moreover, the patent strongly suggests that they are the same. For example, not only are they described using the same terminology – "alloyable metal" – but the patent goes on to state: "The two substrates are then heated to *the melting point* of alloyable metal contacts 214, 216, and 340, 342, and 344, e.g., about 400° C., and then maintained at that temperature for a time period sufficient to metallurgical bond the metal contacts together, i.e., usually for just a few seconds." (Col. 11, lines 60 – 65; emphasis added.) Thus, the patent specifies that there is a *single* melting point of the alloyable metal contacts – thus, that they are made of the same material. There is nothing in the patent which suggests the use of different materials as required by claim 10.

Nor would it be obvious to modify the two-substrate structure of Rostoker so as to provide all of the elements of claim 10 on a single substrate. Specifically, Rostoker emphasizes the advantages of using two substrates, and there is no suggestion or motivation for combining them into one substrate.

CONCLUSION

For the foregoing reasons it is respectfully submitted that all of the pending claims, as amended, are in condition for allowance, and such action is earnestly solicited. The examiner is invited to call the undersigned at the below listed number if there are any remaining questions, or if such action might advance the prosecution of this application.

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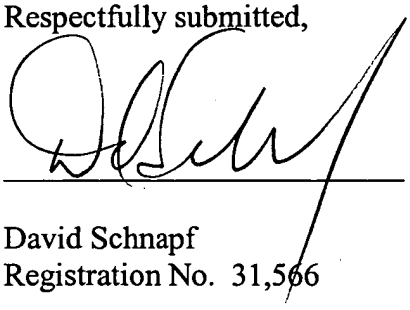
Respectfully submitted,



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